# Architecture of 8051

**Micro Controller :-** It is a device which is used to process the data. It contains a microprocessor, input/output ports, timers and memory integrated on a single IC.

## 1.1 Features of Micro controller

→ It is an 8 bit micro controller
→ It is a 40 pin IC
→ 8 data lines, 16 address lines
→ Interrupt lines - 2
→ Input / output lines - 32
→ Registers - 34 (8 bit), 2 (16 bit)
→ Timers or counters - 2 (16 bit)
→ serial port - 1
→ parallel port - 4
→ Internal ROM - 4KB
→ Internal RAM - 128 Bytes
→ External ROM and RAM - 64KB
→ Operating frequency - 12MHz

## 1.2 Comparision of Microprocessor and Micro controller

| Microprocessor | Micro controller |
|---|---|
| → It contains CPU, RAM, ROM, Timers, I/P & O/P devices are separately interfaced. | → CPU, RAM, ROM, I/O ports and timers all are fabricated on a single chip. |
| → High cost | → Low cost |
| → High power consumption | → Low power consumption. |
| → More Instructions. | → It has less instructions |
| → Complex to design | → Easy to design. |

| Microprocessor | Micro controller |
|---|---|
| → It contains less number of registers | → It contains more number of registers |
| → Speed of operation is low | → Speed of operation is high |
| → Instruction set is complex | → Instruction set is simple |
| → It has general purpose registers | → It has special purpose registers. |
| → It is used in personal computers | → It is used in washing machine. |

1.3 Details of 8051 Microcontroller family chips

| Features | 8051 | 8052 | 8031 |
|---|---|---|---|
| ROM (on chip) | 4 KB | 8 KB | 0B |
| RAM (on chip) | 128 bytes | 256 bytes | 128 bytes |
| Timer / counter | 2 | 3 | 2 |
| Serial port | 1 | 1 | 1 |
| i/o pins | 32 | 32 | 32 |
| Interrupt | 6 | 8 | 6 |

1.4 Functional Block diagram of 8051 Micro controller

The 8051 is a 40 pin IC with NMOS technology the function of each block is

→ Accumulator :- It is a register which contains one of the operand and stores the result of the arithmetic and logic operations.

→ B Register :- It is used to store one of the operands for multiply and divide operations.

→ program status word (PSW) :- It is used to indicate the status of the result. It has 4 flags.

→ Arithmetic and logical unit (ALU):- This unit performs 8 bit arithmetic and logical operations over the operands held by the temporary registers Temp-1 and Temp-2

→ program counter:- It is a 16-bit register which is used to hold the address of next instruction to be executed. It increments continuously to point next instruction by using program counter increment

→ Serial Data Buffer:- It contains two 8 bit registers one for write and one for read operations.

→ Timer registers:- It has two 16-bit timer/counter registers. It can also accessed 8-bit as well as 16-bit

→ Control Registers:- These are 6 control registers namely TCON, TMOD, SCON, PCON, IE and IP

→ Timing and control unit:- This unit driver all the necessary timing and control signals required for the internal operation and also controlling the external system bus.

→ Oscillator:- The circuit generates the basic timing clock signal by using crystal oscillator.

→ Instruction Register:- this register fetches the instruction to be executed.

→ ROM and program address register:- ROM is used for store the program code. This provides on-chip EP-ROM and a mechanism to internally address it.

→ RAM and RAM address:- RAM is used to store the data. This provides 128 bytes of internal RAM. and mechanism to address it internally.

→ ports, latches & drivers:- It has 4 ports. port-0, port-1, port-2, port 3 are 8 bit SFR latches. ~~Except~~ Except P1 the remaining port lines will have dual function.

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→ Stack pointer (SP) :- This is a 8-bit register which is used to store the address of top of the stack.

→ Data pointer (DPTR) :- It is a 16 bit register which is used to store the external data memory address. It can be used as two 8 bit registers DPH & DPL.




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→ Register structure of 8051:-

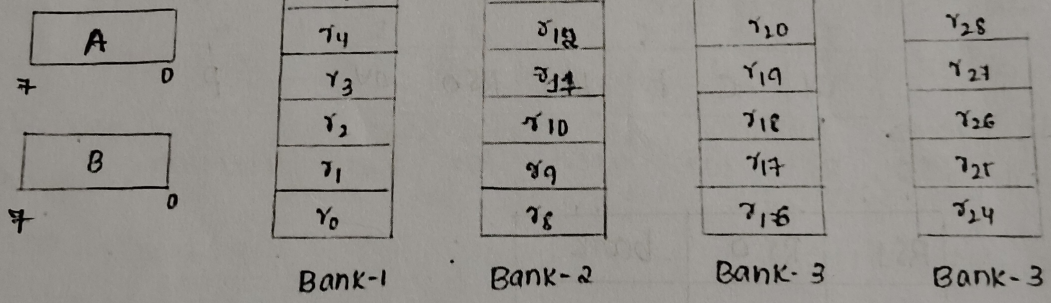
Registers are used to store the data temporarily. The data may be operands and opcode, address of a memory location, address of peripheral.

The 8051 has wide range of registers

* Bit addressable or byte addressable
* general & special purpose
* 8 or 16 bit length

→ General purpose registers:-

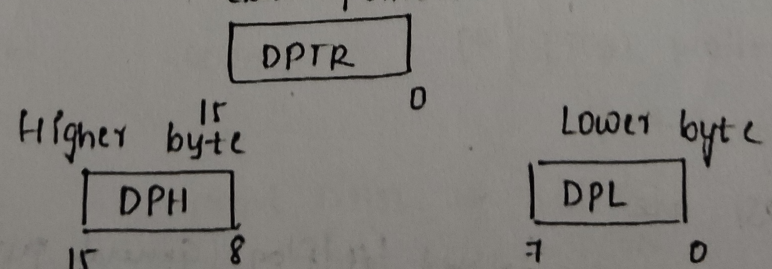
The 8051 has 34 general purpose registers. Those are A, B and remaining 32 are arranged as a part of RAM. These 32 registers are divided into 4 Banks each bank has eight registers.




→ Special purpose registers:-

The 8051 provides 4 special registers they are PC, PSW, DPTR and SP.

→ Data pointer:- It is a 16 bit register It is operated as two 8 bit registers named as DPL and DPH.

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→ Program status word :-

It is a 8 bit register it has 4 flags [carry, Auxilary carry, parity, over flow] and two banks for bank selection of internal RAM

1) Carry flag : The flipflop is forced to SET state whenever there is a carry or barrow generated at $D_7$ bit

2) Auxilary carry flag : The F/F is forced to SET whenever carry is generated from $D_3$ to $D_4$ position.

3) Parity flag :- The F/F is forced to SET whenever the data of accumulator has odd number of logical "1"

4) Over flow flag :- The F/F is forced to SET whenever the result of addition overflows into $D_7$ bit

Arrangement of flags and bank selection bits of PSW.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CY | AC | F0 | RS1 | RS0 | OV | — | P |

* RS0, RS1 are used for bank selection.

| RS1 | RS0 | bank |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

1) P = parity flag

2) OV - over flow flag

3) AC Auxilary carry flag

4) CY - Carry flag

5) RS0 & RS1 are used to select bank

6) F0 is for user defined bit/flag (General purpose flag)

7) $D_1$ bit position - User defined flag

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→ Stack and Stack pointer:

* Stack is used to store the data or address during the execution of a program. Stack pointer is a 8 bit register used to access the stack. It holds the address of top of the stack.
* When data is stored on the stack, the sp value is incremented by one, while retrieving the data from the stack, the sp value is decremented by one. In order to save and retrieve the data PUSH and POP instructions are used.

Special Function Registers (SFR):

* The 8051 has a separate group of registers named as SFR. The accumulator, B register, PSW, DPTR are also comes under this category.
* P0, P1, P2, P3 are 8 bit registers. These are byte addressable and as well as bit addressable.
*. IE and IP are used after the priority among the interrupts and enable the interrupts selectively.
* TH0, TL0, TH1, TL1, TMOD, TCON registers are used to control the funtioning of timer/counters of 8051
* SCON, SBUF are used in serial communication.
* PCON. is used to run the 8051 either in idle mode or power down mode.

| Symbol | Address |
|---|---|
| A | 0E0H |
| B | 0F0H |
| PSW | 0D0H |
| SP | 81H |
| DPL | 82H |
| DPH | 83H |

| Symbol | address |
|---|---|
| P0 | 80H |
| P1 | 90H |
| P2 | 0A0H |
| P3 | 0B0H |
| TMOD | 89H |
| TCON | 88H |
| PCON | 87H |

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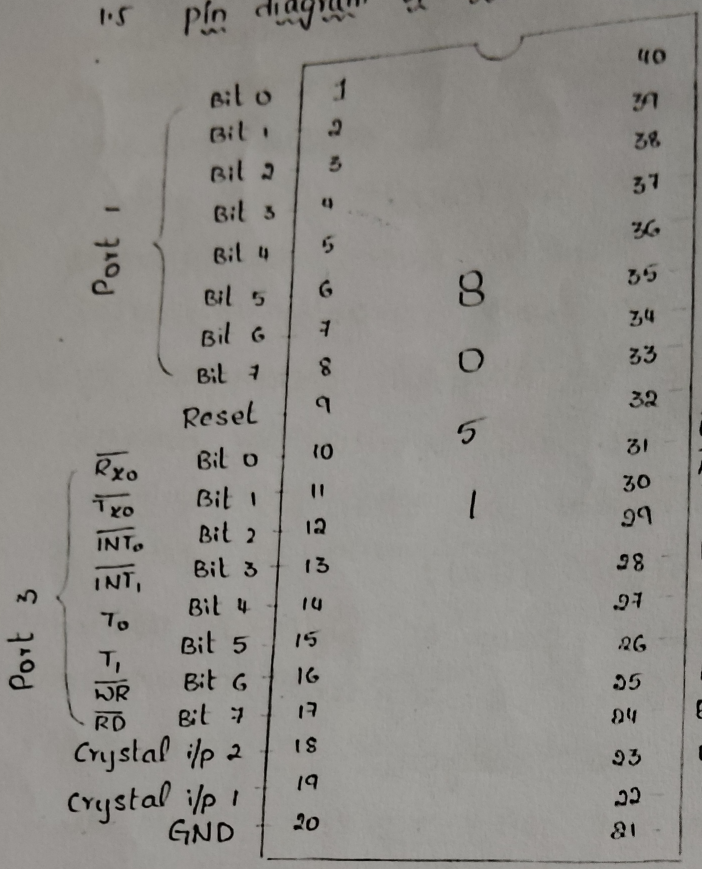
1.5 Pin diagram of 8051 Micro controller




8051 is available in a 40 pin IC [port 1.0 to port 1.7]

* the total lines are 8 named as port-1 and used for input or output from pin 1-8.
* pin 9 [Reset] : Active high input used to reset the MC and terminates all activities
* Pin 10-17 [port 3.0 to port 3.7]. The total 8 lines named as port 3 used for input and output. In addition lines provide special function.
  - → P3.0 (RxD) :- Data received in serial form
  - → P3.1 (TxD) :- Data transmitted in serial form
  - → P3.2 ($\overline{INT0}$) :- Hardware interrupt of location 0003H
  - → P3.3 ($\overline{INT1}$) :- Hardware interrupt of location 0013H
  - → P3.4 (T0) :- pulse input given to timer 0
  - → P3.5 (T1) :- pulse input given to timer 1
  - → P3.6 ($\overline{WR}$) :- memory for write operation
  - → P3.7 ($\overline{RD}$) :- memory for Read operation.

* Pin 20 (GND): This is return pin for the supply. (5)
* Pin 21- 28 : [Port 2.0 to port 2.7] ($A_8$ - $A_{15}$) : The total lines are 8 named as port 2 used for input or output In addition of these lines provides high order address byte.
* Pin 29 : ($\overline{PSEN}$) program store enable is an output pin used to access the external program memory.
* Pin 30 : (ALE) Address Latch Enable is an output pin used to latch the low order address byte ($A_0$- $A_7$) This is for demultiplexing the data and address.
* Pin 31 : ($\overline{EA}$) External ~~address~~ Access is an output pin used to access the external memory.
* Pin 32-39 (P0.0 to port 0.7) ($AD_0$ - $AD_7$). The total pins are 8 named as port 0 and used for input and output. In addition of these lines also provides a dual function carrying of address [low order byte] and data ($D_0$- $D_7$)
* ALE pin indicates these lines are having either address or data
* Pin 40 ($V_{cc}$) : This is a +5V supply voltage pin.
* Internal memory of 8051 :-
* Any, computing device requires memory for program and data.
* program memory (ROM) is used to store the programs to be executed.
* Data memory (RAM) is used to store the data.
* 8051 has internal RAM of 128 bytes and internal ROM. of 4 kilobytes

Internal RAM - 128 bytes

Internal ROM - 4KB

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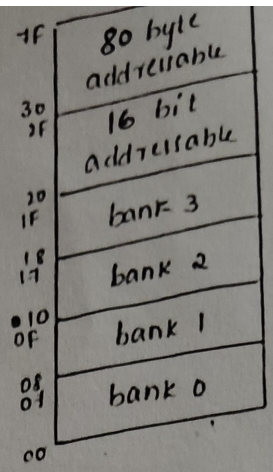
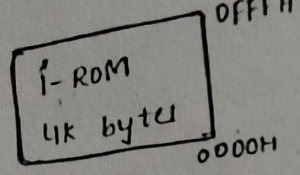
→ Internal RAM (iRAM)

* Internal RAM of 128 bytes.
* Four banks each bank contains 8 registers [00H to 1FH]
* Sixteen bytes are bit addressable [20H to 2FH]
* 80 bytes for general purpose [30H to 7FH]




→ Internal ROM (iROM)

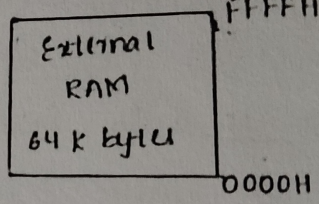
* Internal ROM of 8051 is 4KB
* It ranges from 0000H to 0FFFH
* When the program memory exceeds 0FFFH, it fetch code from external memory.




→ External memory (Off-chip memory)

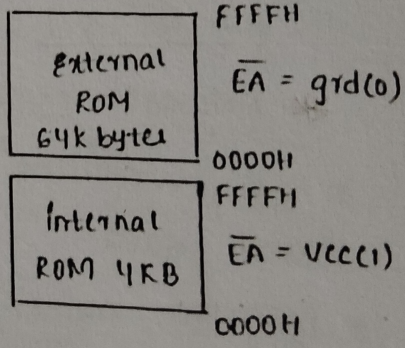
External RAM (RAM)

* External RAM, which is accessed by DPTR
* It address range from 0000H to FFFFH [64KB]




→ External ROM

* A 64KB ROM is also provided to the 8051.
* This memory is used for storing the program codes.
* This memory is accessed by using program counter




* A control pin ($\overline{EA}$) determines the accessing of exact memory i.e either on chip or off chip
* If $\overline{EA}$ = GND then only external (off chip) of 64KB space can be accessed by program counter.

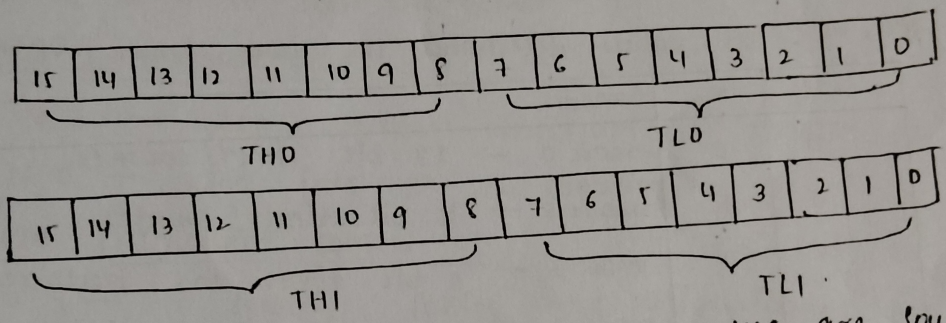
[ $\overline{EA}$ = GND (0)]

If $\overline{EA}$ = Vcc then access on-chip ROM [0000H to 0FFFH] at the end of the on-chip ROM it switches to off chip ROM [1000H to FFFFH]

(6)

* Timers and counters in 8051 associated with SFR's

8051 supports two 16 bit timer registers which can be used as timers as well as counter these two 16-bit timers are divided into two 8 bit timers ~~named~~ as (named) TL0, TH0 and TL1, TH1

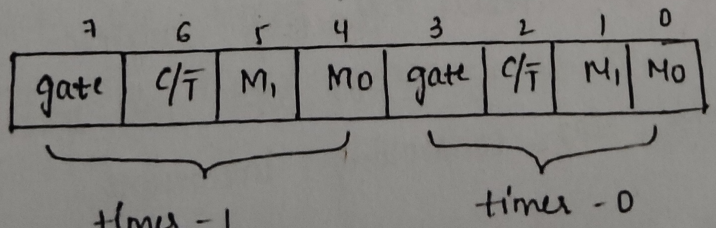



When it used as a timer, the clock pulses are sourced from the oscillator through divide by 12d circuit. When it used as a counter the clock pulses are sourced from the external from P3.4 for counter - 0 and P3.5 for counter - 1

Two SFR's TMOD and TCON are used in timers/counters in order to control their functioning both are 8 bit registers and each bit specifies a specific control.

Timer mode register (TMOD):

TMOD is a 8 bit SFR. It is dedicated to the two timers (T0 & T1) This register is used to determine either it should acts as timer or as counter and mode of working.

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* Lower nibble is used to control timer '0'
* upper nibble is used to control timer '1'

Bit description:

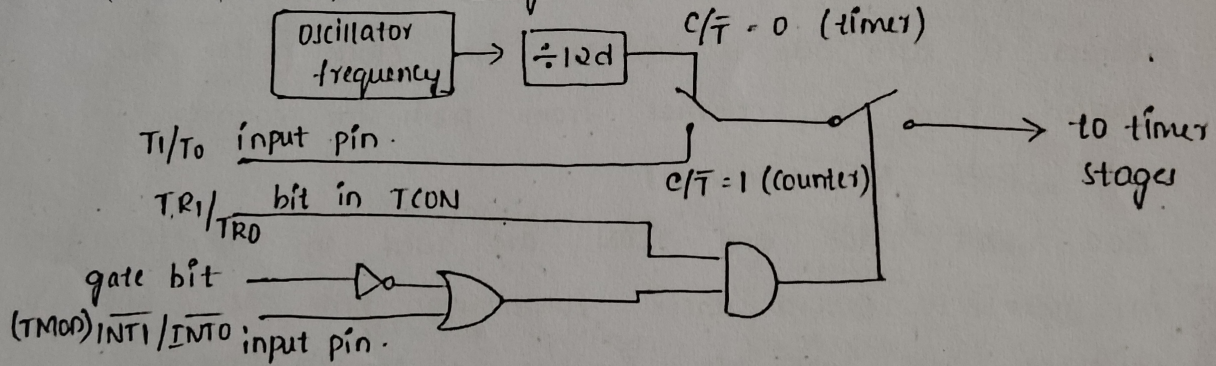
Gate: If gate = 1, the timer/counter is started/stopped using hardware technique.
If gate = 0, start/stop the timer by using software technique.

C/$\overline{T}$: If C/$\overline{T}$ = 1 timer 0/1 acts as counter
If C/$\overline{T}$ = 0 timer 0/1 acts as timer

M0, M1: Bit values determines the mode timer operations

| $M_1$ | $M_0$ | mode |
|---|---|---|
| 0 | 0 | mode 0 → 13 bit timer/counter |
| 0 | 1 | mode 1 → 16 bit timer/counter |
| 1 | 0 | mode 2 → 8 bit timer and auto reload |
| 1 | 1 | mode 3 → two 8 bit timers for timer-0 only |

Timer/counter control logic:




* If C/$\overline{T}$ = 0 it acts as a timer it will count the internal clock frequency of the oscillator.
* If C/$\overline{T}$ = 1 it acts as a counter it will count the external pulse from T1/T0 input pins.

Timer control Register (TCON):-

TCON is a 8 bit special function register the higher nibble is used to turn on or OFF the specific timer the lower nibble for controlling interrupts.

Bit operation :

| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(7)

TF1 / TF0 [over flow flag]

* set to 1 → when the timer rolls from all 1's to all 0's
* set to 0 → over flow flag is disabled.

TR1 / TR0 [ start/ stop]

* set to 1 → to start the timer
* set to 0 → to stop the timer

IE1 / IE0 [ interrupt flag]

* set to 1 → when external interrupt is detected
* set to 0 → when interrupt is processed.

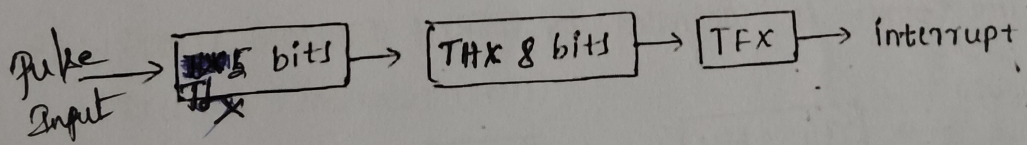
IT1 / IT0 [ Interrupt control Bit]

* set to 1 → to specify falling edge triggering
* set to 0 → to specify low level triggering.

1.11 Modes of operations of counters and timers in 8051.

Mode 0 : [$M_1 = M_0 = 0$]

In this mode the timer can act as 13-bit timer. out of 16 bits 8 bits of $TH_x$ and ~~13 bit timer~~ 5 bits of $TL_x$ are used. under mode 0 the count value could not exceed 'IFFF'H If it reaches the final value it rolls over to 0000H and timer flag [TF 0/1) is raised.




Mode 1 : [$M_1 = 0$, $M_0 = 1$]

In this mode the timer acts as a 16-bit timer In this mode the timer reaches to its maximum value i.e FFFFH, it rolls over to 0000H and TF 0/1 is raised.

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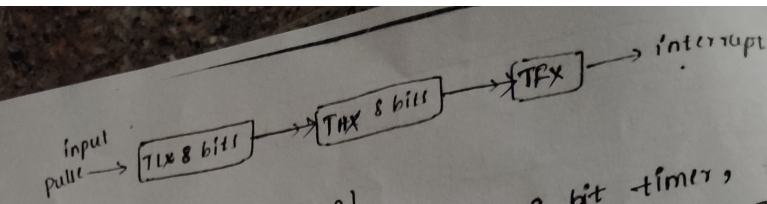
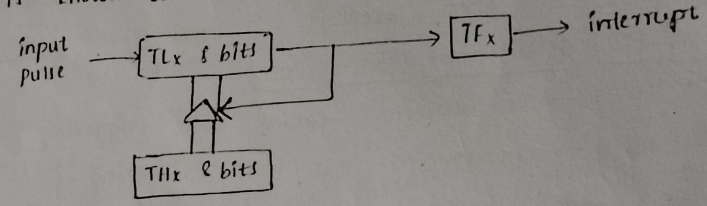



**Mode 2 :** [$M_1 = 1$, $M_0 = 0$]

In this mode the timer acts as 8 bit timer, the THx and TLx are used separately. In this the TLx acts as basic timer. Therefore the count value should not exceed FFH. When timer it will overflow, and will set TFx [timer overflow flag] and reloads the contents of THx to TLx so it is known as auto reload 8 bit them.

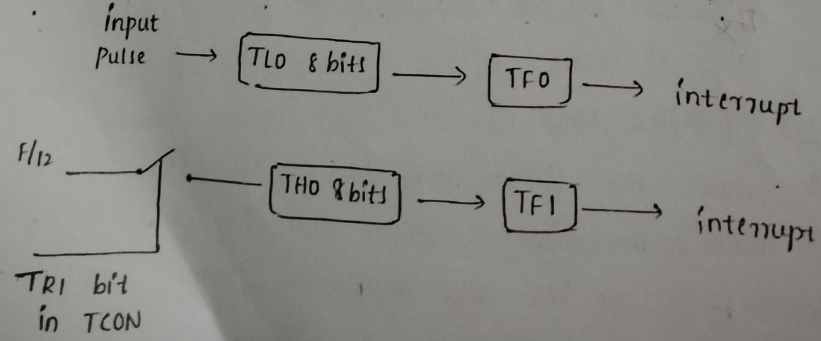



**Mode 3 :** [$M_1 = M_0 = 1$]

It is a special type in which both ~~them~~ timers T0 and T1 do not operate independently like in mode timer -0 acts as two separate 8 bit timers. i.e TL0, TH0.

⇒ TL0 timer is controlled by TR0 & TF0 of TCON bits

⇒ TH0 timer is controlled by TR1 & TF1 of TCON bits.



1.12 Interrupts of 8051 :-

An interrupt is an external or internal event which breaks the mainline sequence of a program. The 8051 μc has five interrupts two external interrupts (INT0, INT1) and 3 internal interrupts (timer interrupts TF0, TF1 and serial port interrupt TI / RI)

Interrupt service routine :

Each interrupt has its own program known as ISR which was stored from a pre determined location. There are 5 locations for the five interrupts fixed by the manufacturer

| | Interrupt | | Address |
|---|---|---|---|
| 1. | External interrupt IE0 | → | 0003H |
| 2. | Timer interrupt TF0 | → | 000BH |
| 3. | External interrupt IE1 | → | 0013H |
| 4. | Timer interrupt TF1 | → | 001BH |
| 5. | Serial interrupt (TI/RI) | → | 0023H |

In order to handle five interrupts the 8051 use SFRS as IE, IP and TCON.

1.13 SFRs associated with interrupts of 8051.

Interrupt priority (IP) : It is a 8 bit SFR. These bits are used to alter the priority among the 5 interrupts the priority of the interrupts is as given below.

1. External interrupt (INT0) highest priority
2. Timer interrupt (TF0)
3. External interrupt (INT1)
4. Timer interrupt (TF1)
5. Serial interrupt (RT/TI) lowest priority.

Bit operation :

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

→ 7 & 6 bits are reversed.

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→ PIL for 8052 only

→ PS : Serial port interrupt
(set to 1 for having highest priority)

→ PT1 : Timer-1 interrupt
(set to 1 for having highest priority)

→ PX1 : External interrupt 1
(set to '1' for having highest priority)

→ PT0 : Timer-0 interrupt
(set to '1' for having highest priority)

→ PX0 : External interrupt-0
(set to '1' for having highest priority)

Interrupt Enable : It is a 8 bit SFR these bits are used to enable or disable the interrupts. It is bit addressable.

Bit description :

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EA | - | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

→ EA : Set to '0' to disable all interrupts
Set to '1' to control all interrupts individually.

→ 6 bit : undefined, kept for future use

→ ET2 :- used by the 8052

→ ET1 : set to '1' to enable timer-1 interrupt

→ ES : Set to '1' to enable serial interrupts.

→ EX1 : Set to '1' to enable external hardware interrupt

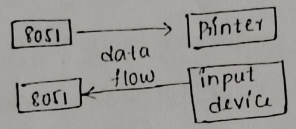
→ ET0 : Set to '1' to enable timer-0 interrupt

→ EX0 : Set to '1' to enable external hardware interrupt.

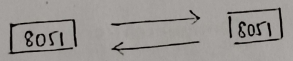
1.14 SFRs associated with serial Communication of 8051 (7)

The 8051 is a 8 bit μc and it transfer 8 bit data simultaneously. In serial input and output mode one bit at a time is transferred over a single line. The serial data communication can be classified according to the direction and simultaneously of data flow.

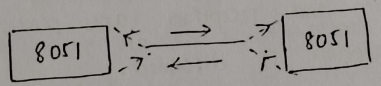
Simplex :- It is a method in which either one device can only tranimit the data. This means that the flow of data will exist in either one direction only.




Duplex :- The data can flow in both the directions at a time It requires two transmission lines




Half duplex : In this only one line will be used but data can flow in both direction at difficult timings




The 8051 has a serial data communication circuit that uses the register SBUF to hold data, register, SCON controls data communication, register PCON controls data rates.

SBUF Register (Serial Port Data Buffer Register)

SBUF is physically two registers of 8 bit each one for write operation used to data. The data to be transmitted out of the 8051 through TxD pin. The other is used read only and holds received data from external source through RxD pin.

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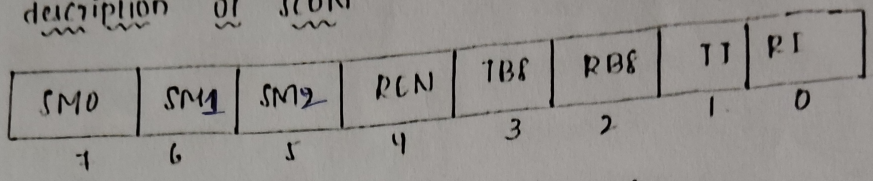
SCON register (Serial Port Control Register):

It is a 8 bit SFR. It is a bit addressable register/ It determines the mode of serial communication and monitors the serial data transfer.

Bit description of SCON




SM0 & SM1 is used for mode selection.

| SM0 | SM1 | mode |
|---|---|---|
| 0 | 0 | → Shift register, baud = f/12 |
| 0 | 1 | → 8 bit UART, variable baud |
| 1 | 0 | → 9 bit UART, baud = f/32 & f/64 |
| 1 | 1 | → 9 bit UART, variable baud. |

→ SM2: Multiprocessor communication bit It is designed for future use to assumed as '0'

→ REN: Set to '1' enable reception i.e if logic 1 both the transmission and reception takes place set to '0' then the reception is disabled.

→ TB8: transmitted bit 8 by program in modes 2 & 3

→ RB8: Received bit 8 it refers bit 8 in mode 2 and 3 stop in mode-1 and not used for mode-0

→ TI: transmit interrupt flag: If it is set to logic '1' for indicating readiness of transmitting next byte If it is '0' to transmit the next byte after loading it into SBUF register.

→ RI: Receiver interrupt flag: If it is set '1' after completing a byte of receiving. If it is '0' for receiving the next byte.

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Baud rate : Speed of Serial transmission is measured in bits per second. baud is defined as the number of bits [number of signal changes] transmitted per second. The normal baud is from 110 to 19200.

PCON : It is a power control register of 8 bit length. It is a byte addressable register.

Bit description :

| SMOD | - | - | - | GF1 | GF0 | PD | IDLE |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

SMOD : Serial baud rate modify bit set to '1' by program to double baud rate using timer-1 for mode 1, 2 and 3. Set to 0' to use timer-1 baud rate.

6-4 : Not implemented.

GF1 : General purpose flag bit '1'

GF0 : General purpose flag bit '0'

PD : Set to '1' to enter power down configuration.

IDLE : Set to '1' to enter Idle mode configuration.

* Input - output pins / ports of 8051 :

The 8051 has a group of 32 I/O pins configured as four 8 bit parallel ports named as P0, P1, P2, P3

All ports are bidirectional

i.e each pin will be configured as input or output.

Each port consists of a latch, an output driver and an input buffer.

When used as input port, '1' must be written to the corresponding port latch by the program i.e (FFH)

When used as output port a '0' must be written to the corresponding port latch by the program i.e (0011)

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Port - 0 :

* Simple input / output port
* The pin numbers of port - 0 is from pin 32 to 39
* Alternate function is bi-directional lower order address data bus for external memory ($AD_0$ to $AD_7$)
* The address of port - 0 is 80H

Port - 1 :

* Simple input / output port
* The pin number of port - 1 is from pin 1 to 8
* this port 1 pins have no dual functions
* The address of port - 1 is 90H

Port 2 :

* Simple input / output port
* The pin number of port 2 is from pin 21 to 28
* The alternate function is higher order address byte ($A_8$-$A_{15}$)
* The address of port - 2 is 0A0H

Port - 3 :

* Simple input / output port
* The pin number of port - 3 is from pin 10 to 17
* Each pin have alternate function.

P3.0 RxD → Receive data serially

P3.1 TxD → transmitt data serially

P3.2 $\overline{INT0}$ → External interrupt 0

P3.3 $\overline{INT1}$ → External interrupt 1

P3.4 T0 → timer - 0

P3.5 T1 → timer - 1

P3.6 $\overline{WR}$ → External memory write pulse

P3.7 $\overline{RD}$ → External memory read pulse

* The address of port - 3 is 0B0H